High On-Off Ratio Bilayer Graphene Complementary Field Effect Transistors

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Abstract

In this paper, we propose a novel S/D engineering for dual-gated Bilayer Graphene (BLG) Field Effect Transistor (FET) using doped semiconductors (with a bandgap) as source and drain to obtain unipolar complementary transistors. To simulate the device, a self-consistent Non-Equilibrium Green's Function (NEGF) solver has been developed and validated against published experimental data. Using the simulator, we predict an on-off ratio in excess of 10^4 and a subthreshold slope of $\sim$110mV/decade with excellent scalability and current saturation, for a 20nm gate length unipolar BLG FET. However, the performance of the proposed device is found to be strongly dependent on the S/D series resistance effect. The obtained results show significant improvements over existing reports, marking an important step towards bilayer graphene logic devices.

Introduction

After the first isolation of Graphene on an oxide substrate, it has attracted a tremendous amount of interest among the researchers due to its extraordinary properties [1]. Using Graphene as the channel material of a FET, that eventually outperforms Si MOSFET, has been one of the major interests in the recent years [2]-[4]. However, in spite of excellent electronic properties [1], suitability for planar MOSFET technology [2], [3] and perfect 2-D electrostatics [4], large area graphene is yet to compete with the existing Si technology in CMOS VLSI due to a lack of significant bandgap, which leads to leaky devices. With the discovery of moderate bandgap opening by the application of a vertical field in a dual-gated BLG structure [5], [6], it has become possible to improve the off state leakage, though the on-off ratio of such transistors are still significantly inferior to Si devices [7]-[10]. In addition to the poor on-off ratio, the small bandgap in the Graphene channel causes a number of issues that need to be overcome before being used as logic devices, namely: (1) There is a lack of sufficient drain current saturation [4], [7], [11]; (2) To control the excessive leakage through the drain barrier, it is required to operate the transistor at low drain bias condition, which in turn adversely affects the on current [7]; and (3) The unipolar devices in Graphene (P-FET and N-FET), which are required to obtain complementary operation in logic circuits, are generally obtained by using charge neutrality point splitting and hence are not very *well-behaved* [12], [13]. In order to address these issues, in the following, we propose a doped semiconductor S/D engineering for BLG FETs which significantly reduces either eletron or hole injection from the S/D contacts by the choice of doping allowing us to obtain unipolar high on-off ratio devices.

Proposed Design

The schematic diagram of a conventional dual-gated BLG FET is shown in Fig. 1(a) where the two gates (G_1, G_2) can be used to control the bandgap and charge in the BLG channel connecting the metal source and drain. As shown in Fig. 1(b) and (c), the BLG channel does not posses any bandgap intrinsically, but a bandgap can be introduced by applying a field through the top and the back gates. A typical transfer characteristics obtained in such a transistor is shown in Fig. 1(d) [7].

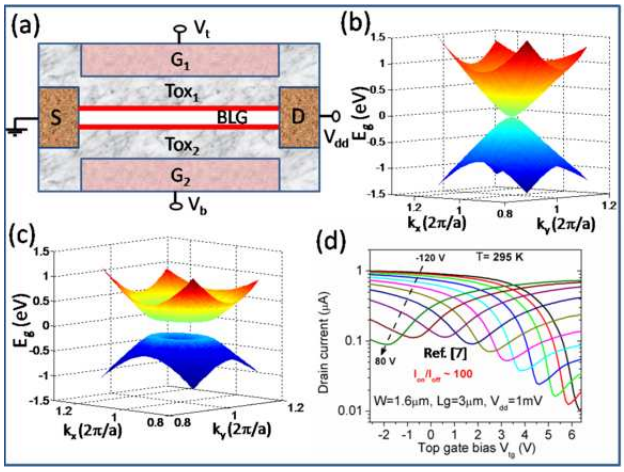

Fig. 1. (a): The schematic of a dual-gated (G_1, G_2) bilayer graphene FET with source (S) and drain (D). (b): Bandstructure of an unbiased infinite BLG film with zero bandgap. (c): Bandgap opening in a *'Mexican hat'* shape under applied external vertical field. (d): Typical experimental transfer characteristics of a metal S/D BLG FET reported in ref. [7] with on-off ratio of $\sim$100 at V_{dd}=1mV and T=295K.

The major off state leakage current paths in such a conventional metal S/D BLG FET are shown in Fig. 2. Since the bandgap (E_g) opened in the channel during off state is not large enough, the source barrier for an electron, which is nearly $E_g/2$, is also small. The barrier for the holes at the drain side is thus even less due to presence of the drain bias V_{dd}. Hence it is difficult to simultaneously reduce the leakage current through both the source barrier and the drain barrier, resulting in poor off state leakage.

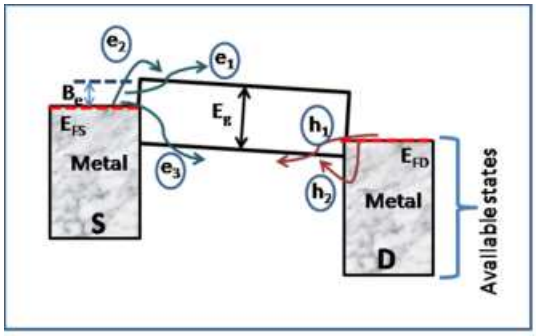

Fig. 2. Schematic band diagram of a conventional metal S/D BLG FET during off state with major leakage paths indicated by arrows. e_1: direct S/D tunneling of electrons; e_2: thermal emission of electrons over source barrier; e_3: source junction tunneling leakage of electrons; h_1: drain junction tunneling leakage of holes; h_2: thermal emission of holes over drain barrier through the available states in the metal. Simultaneous reduction of electron and hole injection to channel is difficult in this device which results in poor on-off current ratio.

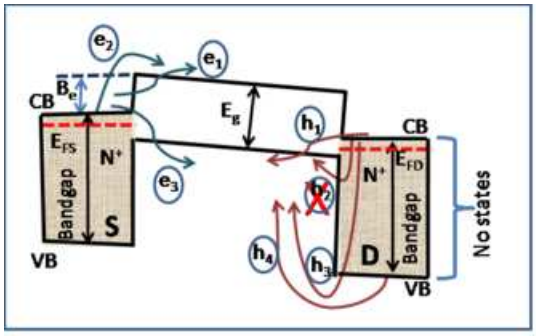

Fig. 3. The leakage paths in the proposed (N^+) doped S/D BLG FET during off state: The thermal emission, h_2, which is generally the major hole leakage component from the drain contact, is no more allowed due to lack of states in the bandgap of the drain. However, the thermal emission h_3 over the bandgap is possible, but is negligible due to the large energy required by the process. Leakage from drain valence band (h_4) is also negligible due to the lack of holes in the valence band of the N^+ doped drain. Reduced hole leakage from the drain in turn allows us to optimize the biasing condition to increase the source barrier B_e reducing e_1 and e_2. However, increasing B_e too much increases tunneling leakage e_3 and h_1 adversely affecting overall off state leakage. We can similarly obtain a BLG P-FET using P^+ doped S/D.

In the proposed solution, as explained in Fig. 3, the metal source and drain are replaced by an N^+ (or P^+) doped semiconductor with a bandgap to obtain a BLG N-FET (or P-FET). We observe in Fig. 3 that the lack of states in the bandgap of the N^+ doped drain significantly reduces the major hole leakage paths. In particular, the thermal hole injection (path h_2) through the drain barrier is completely switched off as the unavailability of states in the bandgap of the drain does not allow this process. The leakages through paths h_3 and h_4 are also almost negligible. The significant reduction of the hole injection from the drain in turn allows us to choose the gate biasing condition such that the electron barrier at the source (B_e) can be significantly increased, helping to suppress the leakage through paths e_1 and e_2 as well. However, excessive pulling up of the source barrier will increase the junction tunneling leakages through paths e_3 and h_1 adversely affecting the total leakage current. Note that, in

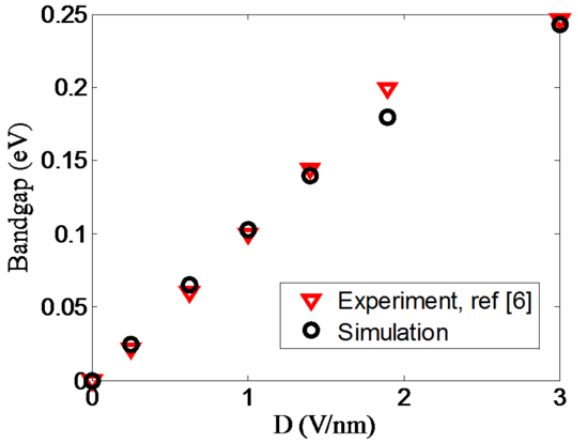

Fig. 4. The simulated external field dependent bandgap of a dual gated BLG film as a function of the displacement vector defined in a similar way as in [6]. There is an excellent agreement with the experimental results reported in [6].

case of conventional metal S/D, this source barrier pulling will aggravate the hole injection from the drain contact and hence can not be used. The reduced hole injection from the drain in the proposed scheme also allows us to operate the BLG FET at higher drain bias, significantly improving the drive current at a given off state current, as compared with metal S/D BLG FETs [7]. Interestingly, the proposed P-FET and N-FET designs are almost symmetric with each other due to the inherent symmetry of the conduction band and the valence band of the BLG channel - an advantage over Si technology. However, in reality, non-identical barrier heights between the BLG channel and the P-type or N-type semiconductor in the source and the drain can introduce asymmetry between the P-FET and the N-FET.

Simulation Method and Validation

We have developed a self-consistent NEGF [9], [10] solver to simulate the proposed dual-gated BLG FET. The device Hamiltonian is constructed by discretizing the real space along the channel length, but a Bloch periodicity is assumed along the width of the channel. The effects of the source and the drain are captured using appropriate self-energy matrices [14]. At every iteration, once the charge distribution is obtained using the LDOS and Fermi statistics, the self-consistent potential is found by solving Poisson equation with appropriate boundary conditions [15]. The real space NEGF simulator takes care of both the thermal as well as the tunneling components of the total drain current. To validate the simulator, in Fig. 4, we find close agreement between the simulated external field dependent bandgap in a BLG film and the corresponding experimental data reported in [6].

We also obtained the on-off current ratios in a metal S/D BLG FET with similar device parameters as in [7]. The simulation predicted numbers are found to be in reasonable agreement with the experimental data, as shown in Fig. 5. In the rest of the paper, we assume a 20nm gate length BLG FET with 1nm equivalent oxide thickness (EOT) at the top

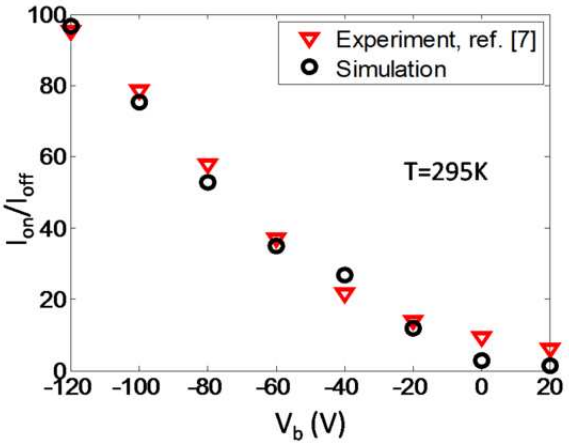

Fig. 5. Simulated on-off current ratio as a function of the back gate bias (V_b) in a similar device as in [7] with L_g=1.6μm and Ti/Pd/Au/Ti S/D at 1mV drain bias. The on state is defined at V_t=$-$2.6 V and off states are the charge neutrality points. The ratios are in good agreement with the experimental results. The minor mismatches can be attributed to the ballistic assumption of the channel in the simulation ignoring scattering. This calibration of the simulation method forms the basis of the results presented in the rest of the paper.

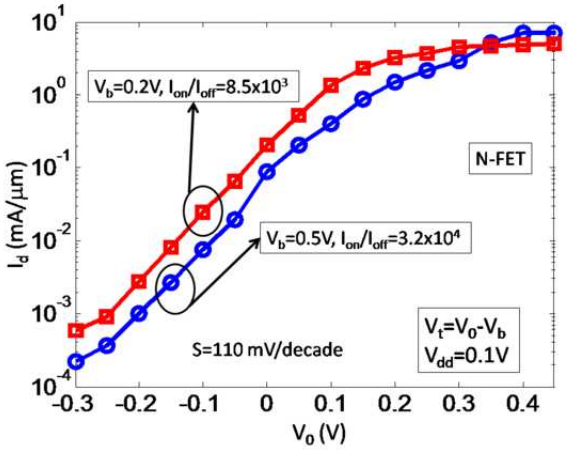

Fig. 6. Transfer characteristics of the proposed BLG FET (N-type) with 20nm gate length, 1nm top and back gate EOT and 0.1V drain bias keeping the bottom gate bias at 0.5V and 0.2V. The former case provides better on-off ratio due to increased bandgap. Both the on-off ratio (3.2×10^4) and the subthreshold slope (S) (110 mV/decade) are the best reported to date for a BLG FET.

and back gates having zero offset bias. The doped source and drain are assumed to have a bandgap of 1.1eV and perfect interface with the channel.

Results and Discussions

The transfer characteristics of the proposed BLG N-FET are plotted in Fig. 6 which show an on-off ratio in excess of 10^4 with a subthreshold slope of nearly 110 mV/decade. Both of these are significant improvements over existing experimental data [7] as well as theoretical predictions [15] for metal S/D BLG FET. This is primarily due to the significant reduction of hole injection through the drain barrier. The transfer characteristics are plotted in the linear scale in Fig. 7

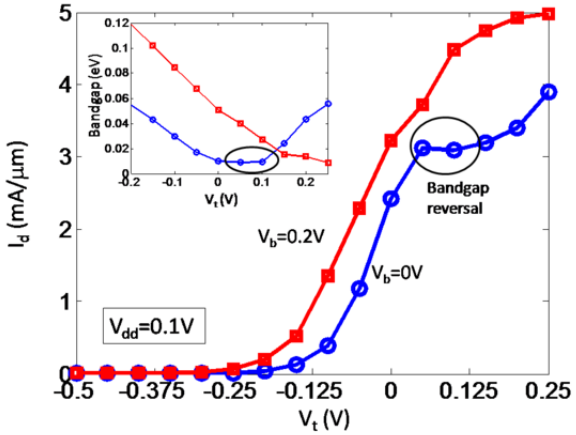

Fig. 7. Transfer characteristics of the proposed BLG FET (N-type) in the linear scale with the back gate kept at 0V and 0.2V. In the former case, a valley is observed in the characteristics due to bandgap reversal effect. Inset: The change in bandgap of the BLG channel as a function of the top gate bias for the two cases.

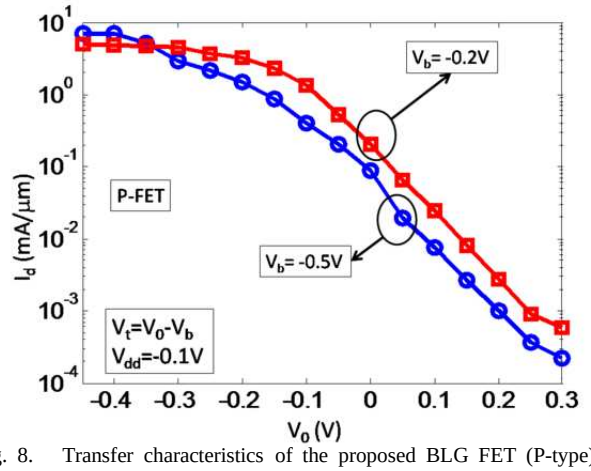

Fig. 8. Transfer characteristics of the proposed BLG FET (P-type) with 20nm gate length and $-$0.1V drain bias keeping the back gate at $-$0.5V and $-$0.2V. The characteristics is similar to the N-FET arising from inherent symmetry of the conduction band and the valence of the BLG channel. This is an advantage over the existing Si technology where symmetry between NMOS and PMOS is obtained by sizing of transistors.

which clearly shows a valley for V_b=0. This is essentially due to the fact that the rate of change of the BLG bandgap changes its sign close to V_t=0, as shown in the inset. In Fig. 8, we plot the transfer characteristics for a BLG P-FET. The observed similarity between the P-FET and the N-FET characteristics reflects the quasi-symmetric conduction band and valence band in the Graphene channel. Here it is important to note that we have assumed similar barrier height characteristics between the BLG channel and the P-type or N-type doped semiconductor S/D.

In Fig. 9, we notice that with an increase in drain bias, there is a drastic degradation in the on-off ratio in the case of metal S/D due to significant lowering of the drain barrier height for holes (path h_2 in Fig. 2). This forces us to operate the FET at low drain bias which in turn degrades the drive current. However, this issue can be potentially solved by using doped S/D which eliminates leakage through path h_2 anyway (Fig.

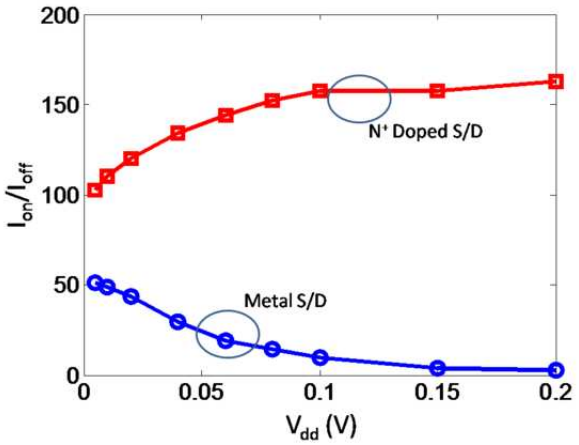

Fig. 9. On-Off ratio as a function of drain bias shows significant degradation of metal S/D BLG FET due to an increase in the hole injection from the drain contact. In case of the doped N^+ S/D, the problem is resolved by the bandgap of the drain and we observe an increase in the on-off ratio with drain bias. Ability to operate the FET at larger drain bias in turn improves the on current significantly. In both cases, the on and off conditions are defined as $V_t = V_b = 0.5$V and $V_t = -V_b = 0.5$V respectively. Note that, the off state is defined in this way for a fair comparison between the two cases and is certainly not optimum for the doped S/D FET.

3). The output characteristics in Fig. 10 show good saturation of the drain current and this consequently enable us to improve gain and noise margin in digital logic as well as gain in RF applications.

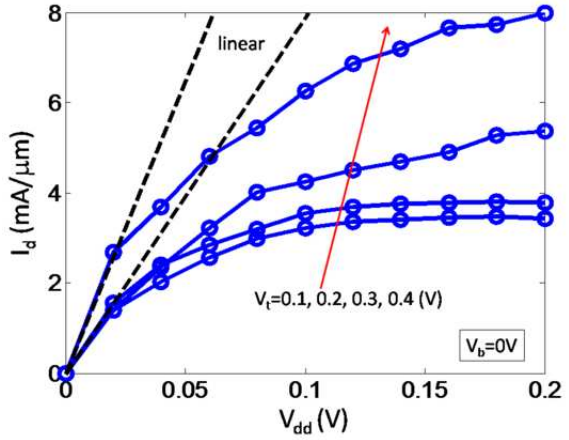

Fig. 10. Output characteristics of the proposed BLG FET show improved saturation of drain current with drain bias. The dotted lines represent the resistor characteristics (linear Ohm's law).

In Fig. 11(a), the on current is plotted against on-off current ratio for a gate length of 15nm and 20nm of the proposed device and is compared against state of the art Si technology. The S/D series resistances are added for realistic performance evaluation and are found to play a key role in determining both the drive current and the on-off ratio. Note that, unlike Si MOSFET, the limit of the subthreshold slope (S) in the proposed BLG FET primarily arises from the intrinsic bias dependence of the electronic structure of BLG [15], and not much from the gate length scaling, due to its ultra-thin structure. This fact plays an important role in determining the scalability of the proposed BLG transistor.

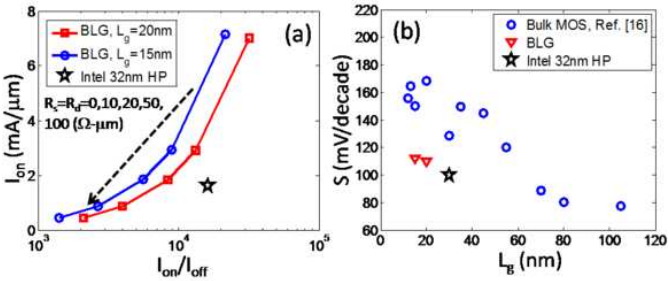

Fig. 11. (a): The on current of the proposed device plotted as a function of on-off ratio shows excellent scalability down to 15nm gate length and compares very well with state of the art Si MOSFET technology. The parasitic series resistances at S/D ($R_{s,d}$) are added for realistic performance comparison. Reduction of $R_{s,d}$ plays a key role in maintaining the high drive current provided from the intrinsic device. (b): Subthreshold slope (S) remains almost the same for both 20nm and 15nm gate length device showing scaling potential of the proposed device due to its ultra-thin structure. However, driving S closer to Boltzmann limit is difficult due to the intrinsic bias dependence of the BLG bandstructure [15]. This scalability is promising when compared with existing state of the art Si technology [16].

This is reflected in Fig. 11(b), where the plotted subthreshold slopes, though are well above the Boltzmann limit, show negligible degradation with gate length providing excellent scalability. The computed subthreshold slopes are found to compare very well with Si MOSFET technology.

Conclusion

In conclusion, we have proposed a doped semiconductor S/D engineering scheme to obtain complementary unipolar BLG FETs. A self-consistent NEGF simulator has been developed and validated against published experimental data to predict the device characteristics. The obtained unipolar characteristics show significant improvement of on-off current ratio, subthreshold slope and drain current saturation over existing published data. The proposed transistor characteristics compare well with state of the art Si technology – marking an important step toward bilayer graphene logic devices.

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